

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chia-Chung Wang et al.

Assignee: Bridge Semiconductor Corporation

Title: METHOD OF MAKING A SEMICONDUCTOR CHIP
ASSEMBLY WITH A CONDUCTIVE TRACE AND A
SUBSTRATE

Serial No.: Unknown Filed: Herewith

Examiner: Unknown Group Art Unit: Unknown

Atty. Docket No.: BDG018

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Pursuant to Applicant's duty of disclosure under 37 C.F.R. § 1.56 and §§ 1.97-1.98, Applicant hereby provides the enclosed Form PTO-1449.

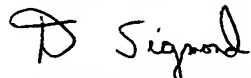
Copies of the documents on the attached Form PTO-1449 are not enclosed because they were previously submitted to or cited by the U.S. Patent Office in U.S. Application Serial No. 09/962,754 filed September 24, 2001, U.S. Application Serial No. 09/878,626 filed June 11, 2001 and/or U.S. Application Serial No. 09/687,619 filed October 13, 2000.

The above-identified application is a continuation-in-part of the '754 application, which is a continuation-in-part of the '626 application, which is a continuation-in-part of the '619 application. Therefore, the documents need not be resubmitted in order to be considered by the Examiner. See M.P.E.P § 609.

The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, an admission that any of these documents, alone or in

any combination, is considered to be material to patentability, an admission that any of these documents is prior art as to the above-identified application, or an admission against interest in any manner.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "D. Sigmond". The signature is written in a cursive, flowing style.

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| Form PTO-1449 U.S. Department of Commerce, Patent and Trademark Office | | | | | Atty Docket No. BDG018 | | Serial No. | |
| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | | | | | Applicant Chia-Chung Wang et al. | | | |
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| | AP | U.S. Application Serial No. 09/464,562, filed December 16, 1999, entitled "Bumpless Flip Chip Assembly With Strips And Via-Fill" | | | | | | |
| | AQ | U.S. Application Serial No. 09/464,561, filed December 16, 1999, entitled "Bumpless Flip Chip Assembly With Strips-In-Via And Plating" | | | | | | |
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| | | | | | | | Translation | |
| | | Document | Date | Country | Class | Subclass | Yes | No |
| | AN | | | | | | | |
| | AO | | | | | | | |
| Other Art (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | | |
| | AP | | | | | | | |
| | AQ | | | | | | | |
| Examiner | | | Date Considered | | | | | |
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|--|----|--------------------|-----------------|-----------------|-------------------------------------|----------|-------------------------------|----|
| Form PTO-1449 U.S. Department of Commerce, Patent and Trademark Office | | | | | Atty Docket No. BDG018 | | Serial No. | |
| INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) | | | | | Applicant Chia-Chung Wang et al. | | | |
| | | | | | Filing Date | | Group Art Unit | |
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| Foreign Patent Documents | | | | | | | | |
| | | | | | | | Translation | |
| | | Document | Date | Country | Class | Subclass | Yes | No |
| | AN | | | | | | | |
| | AO | | | | | | | |
| Other Art (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | | |
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| | AQ | | | | | | | |
| Examiner | | | Date Considered | | | | | |
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| Form PTO-1449 | | | | Atty Docket No. | | Serial No. | |
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| U.S. Patent Documents | | | | | | | |
| *Examiner Initial | | Document Number | Date | Name | Class | Subclass | Filing Date If Appropriate |
| | AA | | | | | | |
| Foreign Patent Documents | | | | | | | |
| | | | | | | | Translation |
| | | Document | Date | Country | Class | Subclass | Yes No |
| | AB | | | | | | |
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| | AE | U.S. Application Serial No. 09/643,214, filed August 22, 2000, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" | | | | | |
| | AF | U.S. Application Serial No. 09/643,213, filed August 22, 2000, entitled "Method Of Making A Support Circuit For A Semiconductor Chip Assembly" | | | | | |
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| | AH | U.S. Application Serial No. 09/665,928, filed September 20, 2000, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint" | | | | | |
| | AI | U.S. Application Serial No. 09/665,931, filed September 20, 2000, entitled "Method Of Making A Support Circuit With A Tapered Through-Hole For A Semiconductor Chip Assembly" | | | | | |
| | AJ | U.S. Application Serial No. 09/677,207, filed October 2, 2000, entitled "Method Of Making A Semiconductor Chip Assembly With A Conductive Trace Subtractively Formed Before And After Chip Attachment" | | | | | |
| Examiner | | | Date Considered | | | | |
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| U.S. Patent Documents | | | | | | | |
| *Examiner Initial | | Document Number | Date | Name | Class | Subclass | Filing Date If Appropriate |
| | AA | | | | | | |
| Foreign Patent Documents | | | | | | | |
| | | | | | | Translation | |
| | | Document | Date | Country | Class | Subclass | Yes No |
| | AB | | | | | | |
| Other Art (Including Author, Title, Date, Pertinent Pages, Etc.) | | | | | | | |
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| | AD | U.S. Application Serial No. 09/864,555, filed May 24, 2001, entitled "Semiconductor Chip Assembly with Simultaneously Electrolessly Plated Contact Terminal and Connection Joint" | | | | | |
| | AE | U.S. Application Serial No. 09/864,773, filed May 24, 2001, entitled "Semiconductor Chip Assembly With Ball Bond Connection Joint" | | | | | |
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